What Is Claimed Is:

1. A wafer having a surface, the wafer comprising:

a plurality of regions of semiconductor and dielectric exposed at the surface of the wafer after chemical mechanical planarization, wherein the semiconductor regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and each of the semiconductor regions have a shortest surface dimension that is less than or equal to a first width, the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

2. The wafer of claim 1 wherein the first fraction equals 60%.

3. The wafer of claim 1 wherein the first fraction equals 50%.

4. The wafer of claim 1 wherein the first width equals 2.5 millimeters.

5. The wafer of claim 1 wherein the first width equals 500 microns.

6. The wafer of claim 1 wherein the semiconductor regions comprise silicon.

7. The wafer of claim 1 wherein the dielectric regions comprise silicon dioxide.

8. The wafer of claim 1 wherein the regions of dielectric and semiconductor alternate along the surface of the wafer.

9. The wafer of claim 1 wherein the regions of dielectric are elongated strips.

10. The wafer of claim 1 wherein the regions of semiconductor are elongated strips.

11. The wafer of claim 1 wherein the regions of dielectric are rectangular.

12. The wafer of claim 1 wherein the regions of semiconductor are rectangular.

13. The wafer of claim 1 wherein the regions of semiconductor are hexagonal.

14. The wafer of claim 1 wherein the regions of semiconductor are interspersed within a sea of dielectric.

15. A method for cleaning a surface of a wafer, comprising:

depositing a semiconductor layer and a dielectric layer;

removing portions of the semiconductor layer or the dielectric layer using chemical mechanical planarization to expose surfaces of dielectric and semiconductor regions, wherein the semiconductor regions have a combined surface area that is less than or equal to a first fraction of a surface area of the wafer and each of the semiconductor regions has a

shortest surface dimension that is less than or equal to a first width; and

cleaning the wafer surface using a wet clean technique to remove residual particles therefrom.

16. The method of claim 15 wherein the first fraction equals 60%.

17. The method of claim 15 wherein the first fraction equals 50%.

18. The method of claim 15 wherein the first width equals 2.5 millimeters.

19. The method of claim 15 wherein the first width equals 500 microns.

20. The method of claim 15 wherein the semiconductor regions comprise silicon.

21. The method of claim 15 wherein the dielectric regions comprise silicon dioxide.

22. The method of claim 15 wherein the regions of dielectric and semiconductor alternate along the surface of the wafer.

23. The method of claim 15 wherein the regions of dielectric are elongated strips.

24. The method of claim 15 wherein the regions of semiconductor are elongated strips.

25. The method of claim 15 wherein the regions of dielectric are rectangular.

26. The method of claim 15 wherein the regions of semiconductor are rectangular.

27. The method of claim 15 wherein the regions of semiconductor are hexagonal.

28. The method of claim 15 wherein depositing the semiconductor layer and the dielectric layer comprises first depositing the semiconductor layer, selectively masking and etching the semiconductor layer, and subsequently depositing the dielectric layer over the semiconductor layer.

29. The method of claim 15 wherein the regions of semiconductor are interspersed within a sea of dielectric.

30. A wafer having a surface, the wafer comprising:

means for attracting water to the surface of the wafer; and

means for repelling water from the surface of the wafer comprising regions that have a combined surface area that is less than or equal to a first fraction of a surface area of the wafer,

wherein each of the regions has a shortest surface dimension that is less than or equal to a first width, and the first fraction and the first width ensure that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

31. The wafer of claim 30 wherein the first fraction equals 60%.

32. The wafer of claim 30 wherein the first fraction equals 50%.

33. The wafer of claim 30 wherein the first width equals 2.5 millimeters.

34. The wafer of claim 30 wherein the first width equals 500 microns.

35. The wafer of claim 30 wherein the means for repelling water comprises silicon.

36. The wafer of claim 30 wherein the means for attracting water comprises silicon dioxide.

37. The wafer of claim 30 wherein the means for attracting water comprises elongated strips of dielectric.

38. The wafer of claim 30 wherein the means for attracting water comprises of rectangular regions of dielectric.

39. The wafer of claim 30 wherein the means for attracting water comprises dielectric regions, the means for repelling water comprises semiconductor regions, and wherein the dielectric regions and semiconductor regions alternate along the surface of the wafer.

40. The wafer of claim 30 wherein the means for repelling water comprises elongated strips of semiconductor.

41. The wafer of claim 30 wherein the means for repelling water comprises rectangular regions of semiconductor.

42. The wafer of claim 30 wherein the means for repelling water comprises hexagonal regions of semiconductor.

43. The wafer of claim 30 wherein the means for attracting water comprises dielectric, the means for repelling water comprises semiconductor regions, and the semiconductor regions are interspersed within a sea of dielectric.

44. A wafer having a surface, the wafer comprising:

a plurality of regions of hydrophobic material and hydrophilic material exposed at the surface of the wafer after chemical mechanical planarization, wherein the regions of hydrophobic material have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and each of the regions of hydrophobic material have a shortest surface dimension that is less than or equal to a first width, the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

45. The wafer of claim 44 wherein the first fraction equals 60%.

46. The wafer of claim 44 wherein the first fraction equals 50%.

47. The wafer of claim 44 wherein the first width equals 2.5 millimeters.

48. The wafer of claim 44 wherein the first width equals 500 microns.

49. The wafer of claim 44 wherein the hydrophobic material comprises silicon.

50. The wafer of claim 44 wherein the hydrophilic material comprises silicon dioxide.

51. The wafer of claim 44 wherein the regions of hydrophobic material and hydrophilic material alternate along the surface of the wafer.

52. The wafer of claim 44 wherein the regions of hydrophilic material and hydrophobic material are elongated strips.

53. The wafer of claim 44 wherein the regions of hydrophilic material are rectangular.

54. The wafer of claim 44 wherein the regions of hydrophobic material are rectangular.

55. The wafer of claim 44 wherein the regions of hydrophobic material are hexagonal.

56. The wafer of claim 44 wherein the regions of hydrophobic material are interspersed within a sea of hydrophilic material.